Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTIONS:**

1. **OUTPUT**
2. **COMMON**
3. **INPUT**

**.052”**

**.044”**

**2 1**

**3**

**UA78L**

**MASK**

**REF**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .0038” min.**

**Backside Potential: Common**

**Mask Ref: UA78L**

**APPROVED BY: DK DIE SIZE .044” X .052” DATE: 4/27/23**

**MFG: TEXAS INSTRUMENTS THICKNESS .010” P/N: UA78L15**

**DG 10.1.2**

#### Rev B, 7/19/02